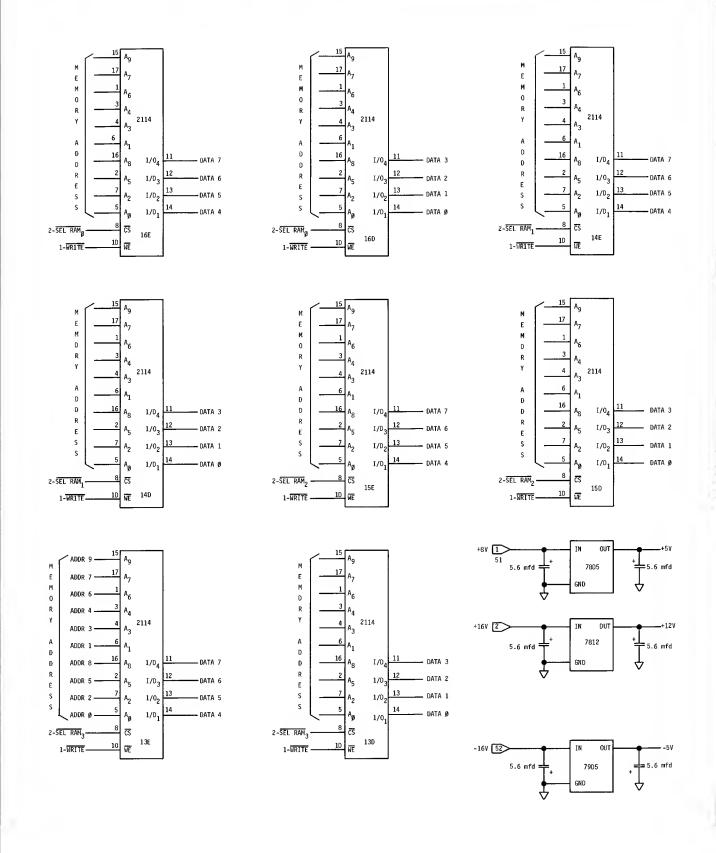


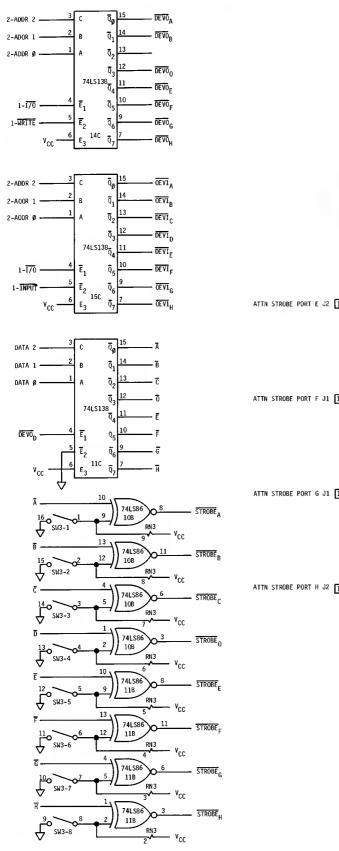
THE SWITCHBOARD - S-100 1/0 INTERFACE REVISION 2

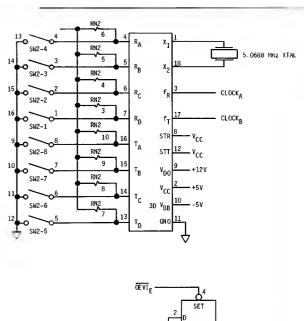
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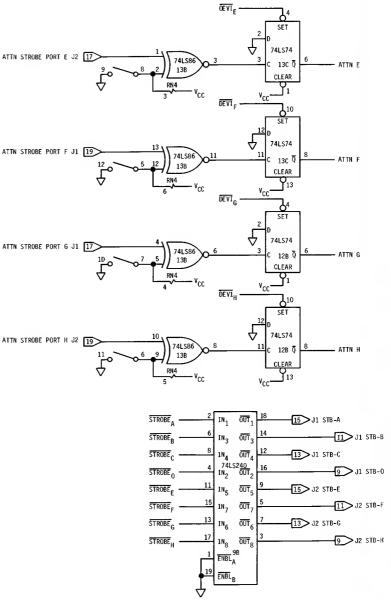
ADDRESS & INPUT DATA BUFFERS, ROM, AND MEMORY SELECT LOGIC



REVISION 2







THE SWITCHBOARD - S-100 I/O INTERFACE REVISIÓN 2

I/O SELECT, STROBE SELECT & BUFFERS, AND SERIAL CLOCK LOGIC

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